REMARKS

I. Introduction

In response to the Office Action dated March 2, 2006, Applicants respectfully request reconsideration of the pending rejection for the reasons set forth below.

II. Claim Rejections Under 35 U.S.C. § 103

Claims 1-8 and 11 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,886,152 to Kong in view of USP No. 5,687,088 to Tomita. Applicants submit that this rejection is in error for at least the following reasons.

As discussed in a previously filed response, the present invention relates to a method for designing a semiconductor circuit which allows for the reduction in the power consumption of the resulting circuit. Specifically, the method of the present invention allows for *the insertion of a load-dividing buffer* ***at a position subsequent to a branching point*** and for the reduction of the drive capability of the drive cell disposed preceding the branching point. As a result of this process, excessive design margins provided for drive cells located prior to branching points, which were provided in order to satisfy timing constraints of a given line of the multiple lines associated with the given branching point, can be reduced, as the newly inserted load-dividing buffer can drive the critical line, and the drive cell (now having reduced design margin) can drive the non-critical lines associated with the given branching point. A specific example of the method of the present invention is set forth in paragraphs [0048] to [0052] of the specification.

Turning to the claims, claim 1 recites in-part the steps of: (1) detecting a branch point of a wire in the layout; (2) ***virtually inserting a load at a predetermined point on one of the wires subsequent to the detected branching point***; (3) ***calculating a delay amount of each route connecting cells via the branching point with the load being inserted and a delay amount***

without the load being inserted; (4) ***determining, based on the delay amount of each route, an insertion point at which a load-dividing buffer is to be inserted***; (d) calculating a drive capability of a driving cell preceding the insertion point, and (e) ***deciding whether the load-dividing buffer is insertable at the insertion point.***

Turning to the cited prior art references, it is respectfully submitted that Kong wholly fails to disclose or suggest any of the limitations that the pending Office Action asserts Kong discloses. Kong is related to a method for determining a satisfactory routing layout. There is no mention or suggestion in Kong of attempting to reduce the design margins of the drive cells utilized in the circuit design. One of the main objectives of the routing process of Kong is to route or re-route all of the non-critical loads through the driver with the largest "slack" (i.e., available drive capacity), *see*, col. 6, lines 50-59 of Kong. The "branching penalties" of Kong appear to be assigned values to wire segments, which can be arbitrarily assigned by the router, and which are utilized to determine which nodes critical and non-critical segments will be routed through, *see*, col. 6, lines 59-65 of Kong. Kong does not disclose or suggest any method of reducing the power requirements of the drive cells contained within the design by insertion of load-dividing buffers. In this regard, it is noted that the present invention could be utilized after the routing layout process has been completed, whereas Kong is specifically directed at a routing layout process.

In the pending Office Action, it is asserted that Kong's process of attempting to determine if different routing layouts provide a more optimal result corresponds to the recited insertion of a virtual load. Clearly, it does not. As recited by claim 1, *delay amounts for each routing line subsequent to the branching point* ***are calculated with and without the load.*** It cannot be properly concluded that the step of attempting different routing layouts as disclosed in

Kong meets this limitation. It simply does not, as there is no correlation between the two. Kong does not perform any such calculation. Moreover, in the present invention, *the loads are virtually inserted* ***subsequent to branching points***. Kong doesn't appear to mention inserting anything subsequent to branching points, much less performing the recited calculations noted above.

It is noted that the foregoing steps are part of the claimed process for determining if an additional load-dividing buffer is necessary and can be inserted in a routing line subsequent to a given "branch" point. The portion of Kong (col. 5, lines 16-20) cited as corresponding to this element merely discloses that all non-critical routing lines should be routed through a single buffered PIP. This is wholly unrelated to the foregoing process steps recited by claim 1.

Tomita does not cure any of the deficiencies of Kong. Tomita relates to a simulation process that allows for more accurate simulation of the delay associated with node connections in a layout. More specifically, in order to simulate a margin of transition delay occurring due to capacitive coupling between adjacent wires (i.e., node connections), delay adding means (i.e., loads) are provided for the node connections to represent the transition delay assumed to occur (*see*, Tomita, col. 5, lines 17-35). Importantly, however, similar to Kong, Tomita is silent with regard to inserting such loads subsequent to branching points or calculating delay amounts for each routing line subsequent to the branching point with and without the load. Furthermore, Tomita merely discloses a process for improving simulation results. There is no disclosure or suggestion in Tomita that the delay adding means disclosed therein can be utilized in a process to add load-dividing buffers to the actual layout.

Thus, even assuming *arguendo* that Kong and Tomita were properly combinable, the combination of Kong an Tomita still fails to disclose the foregoing elements recited by claim 1.

As each and every limitation must be disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (M.P.E.P. § 2143.03), and the combination of Kong and Tomita clearly fails to do so, it is respectfully submitted that claim 1 is patentable over Kong and Tomita taken alone or in combination with one another. It is also submitted that claim 11 is patentable over the cited prior art for at least the same reasons as discussed above.

It is well known that the fact that the prior art could be modified so as to result in the combination defined by the claims at bar would not have made the modification obvious unless the prior art suggests the desirability of the modification. ***In re Deminski***, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).

Moreover, recognizing after the fact that such a modification would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. ***In re Warner***, 379 F.2d 1011, 154, USPQ 173 (CCPA 1967).

Indeed, it is only Applicants' disclosure that discloses a process in which a delay amount of each route connecting cells to a branching device is calculated with the virtual load inserted in the route and without the virtual load being inserted, and in which load-dividing buffers (which change the actual layout configuration of the device) are placed in some routes based the results of these calculations. As explained above, both Kong and Tomita appear silent regarding these elements of the claims. Moreover, neither Kong nor Tomita appear to acknowledge the problems solved by the present invention. Thus, the only motivation of record for the proposed modification of the device of Kong and Tomita to arrive at the claimed invention is found in Applicants' disclosure which, of course, may not properly be relied upon to support the ultimate legal

conclusion of obviousness under 35 U.S.C. §103. ***Panduit Corp. v. Dennison Mfg. Co.***, 810 F.2d 1561, 227 1 USPQ2d 1593 (Fed. Cir. 1987).

Reliance upon "general knowledge" (of what is known) to reject claims is not objective evidence that claims as a whole, are obvious within the meaning of 35 U.S.C. § 103. In addition, mere conclusions that various aspects of the claimed invention are obvious does not support a ***prima facie*** case of obviousness under 35 U.S.C. § 103. In this regard, Applicants stress that what may be known in some general context does not necessarily render the claimed subject matter as a whole obvious within the meaning of 35 U.S.C. § 103.

For all of the foregoing reasons, it is respectfully submitted that pending claims are patentable over Kong and Tomita taken alone or in combination with one another.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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